AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A switch matrix circuit comprising:

a plurality of switches organized in a row and column configuration; and

a current sensing circuit coupled to the plurality of switches, the current sensing circuit including a transistor ~~and at least one resistor~~ per column of the plurality of switches, and a plurality of resistors each electrically coupled in series with an associated one of the plurality of switches, wherein current amplified by the transistor ~~and converted by the at least one resistor~~ in a column is sensed as a logic state indicative of a switch status of a switch within the column for a selected row, and wherein the column is configured to conduct at least a threshold current level required for the transistor to perform the amplification if the switch is closed, and to conduct less than the threshold current level if the switch is open, regardless of how many other of the plurality of switches are closed.

2. (Original) The switch matrix circuit of claim 1, wherein the transistor further comprises a bipolar junction transistor.

3. (Original) The switch matrix circuit of claim 1, wherein the row and column configuration further comprises an off-diagonal configuration having one switch per row and column intersection in all but one intersection per row.

4. (Original) The switch matrix circuit of claim 3, wherein each intersection lacking a switch lies in a different column within each row.

5. (Original) The switch matrix circuit of claim 4, wherein a single scan line supports providing a row input signal or reading a column output signal for one row and one column within the off-diagonal configuration.

6. (Original) The switch matrix circuit of claim 1, wherein a processor senses the switch status.

7. (Currently Amended) A circuit for more efficient switch selection sensing, the circuit comprising:

a switch matrix comprising a plurality of switches organized as a plurality of rows and columns;

a current sensing circuit coupled to the switch matrix; and

a processor coupled to the switch matrix and the current sensing circuit by a plurality of scan lines, wherein selection of a single row by a scan line returns column current levels from the current sensing circuit to detect if a switch at an intersection of the single row and a column ~~intersection~~ of the switch matrix ~~has been selected,~~ is closed, and wherein a column current level associated with the column is at least a threshold current level required for detection if the switch is closed, and the column current level associated with the column is less than the threshold current level if the switch is open, regardless of how many other of the plurality of switches are closed.

8. (Original) The circuit of claim 7, wherein the plurality of scan lines further comprise a plurality of bi-directional scan lines wherein a single scan line provides both row selection and column sensing capabilities.

9. (Original) The circuit of claim 8, wherein the organization of the plurality of switches further comprise an off-diagonal organization to support the bi-directional scan lines.

10. (Currently Amended) The circuit of claim 7, wherein the current sensing circuit further comprises a ~~transistor and resistor~~ circuit comprising a plurality of transistors each coupled to an associated column, and a plurality of resistors each coupled in series with an associated one of the plurality of switches ~~for each column~~ in the switch matrix.

11. (Currently Amended) The circuit of claim 10, wherein the column current level[[s]] ~~indicate~~ associated with the column is at least the threshold current level when the transistor coupled to the column is turned on ~~and current passes through the resistor~~.

12. (Original) The circuit of claim 10, wherein the transistor further comprises a bipolar junction transistor.

13. (Currently Amended) A method for sensing switch statuses, the method comprising:

coupling a current sensing circuit to a switch matrix having a plurality of switches in a row and column configuration comprising one switch per row and column intersection; and

~~utilizing a processor to detect~~ detecting a switch status of a switch within the switch matrix based on whether a current signal[[s]] in the current sensing circuit comprises at least a threshold current level, regardless of how many other of the plurality of switches are closed.

14. (Currently Amended) The method of claim 13, further comprising forming the current sensing circuit comprising [[as]] a transistor ~~and at least one resistor~~ per column of the plurality of switches, and a plurality of resistors each electrically coupled in series with an associated one of the plurality of switches.

15. (Currently Amended) The method of claim 14, wherein ~~utilizing a processor to detect~~ detecting the switch status of the switch further comprises detecting current amplified by the transistor ~~and converted by the at least one resistor~~ in a column as a logic state indicative of the switch status of the switch, wherein the switch is located at an intersection of ~~within~~ the column ~~for~~ and a selected row.

16. (Currently Amended) The method of claim ~~15~~ 13, wherein ~~utilizing a processor~~ detecting the switch status of the switch further comprises utilizing a plurality of bi-directional scan lines, wherein a single scan line provides both row selection and column sensing capabilities.

17. (Currently Amended) The method of claim 16, ~~further comprising organizing~~ wherein the plurality of switches [[as]] comprises an off-diagonal organization to support the bi-directional scan lines.

18. (Currently Amended) The method of claim 14, ~~further comprising utilizing~~ wherein the transistor per column of the plurality of switches comprises a bipolar junction transistor ~~as the transistor~~.

19. (Currently Amended) A switch matrix circuit comprising:

a plurality of switches organized in a row and column off-diagonal configuration having one switch per row and column intersection in all but one intersection per row; and

a plurality of ~~scan lines comprising a plurality of~~ bi-directional scan lines, wherein a single bi-directional scan line provides both row selection and column sensing capabilities for switch ~~selection~~ status identification, wherein:

a first bi-directional scan line of the plurality of bi-directional scan lines is configured to conduct a first signal associated with a first logic state to a selected row of the switch matrix coupled thereto;

a second bi-directional scan line of the plurality of bi-directional scan lines is configured to be scanned for an output signal comprising at least a threshold level, wherein the output signal comprises at least the threshold level only if a scanned switch at an intersection of the selected row and a scanned column of the switch matrix is selected, wherein the scanned column is coupled to the second scan line; and

each of the other bi-directional scan lines of the plurality of bi-directional scan lines is configured to conduct a second signal associated with a second logic state opposite the first logic state.

20. (Original) The switch matrix of claim 19, wherein the one intersection per row lacking a switch lies in a different column within each row.

21. (Currently Amended) The switch matrix of claim 19, wherein an analog to digital converter senses a switch status for the scanned switch, wherein a closed switch status is sensed if the output signal comprises at least the threshold level, and an open switch status is sensed if the output signal comprises less than the threshold level.

22. (Original) The switch matrix of claim 19, further comprising a diode and resistor circuit for each scan line.

23. (Currently Amended) A circuit for more efficient switch ~~selection~~ status sensing, the circuit comprising:

a switch matrix including a plurality of switches organized as a plurality of rows and columns; and

a plurality of resistors, each of the resistors electrically coupled in series with an associated one of the plurality of switches;

a voltage threshold sensing circuit coupled to the switch matrix by a plurality of scan lines; and

a processor coupled to the voltage threshold sensing circuit by a signal bus, wherein selection of a selected row by a scan line returns a scanned column voltage level[[s]] from the switch matrix to detect if a switch at an intersection of the selected row and the scanned column ~~intersection~~ of the switch matrix has been selected.

24. (Currently Amended) The circuit of claim 22, wherein the voltage threshold sensing circuit converts the scanned column voltage level[[s]] to a logic state[[s]].

25. (Currently Amended) The circuit of claim 24, wherein the voltage threshold sensing circuit ~~includes~~ comprises an analog to digital converter.

26. (Original) The circuit of claim 24, wherein the voltage threshold sensing circuit includes a voltage level converter including a transistor.

27. (New) The method of claim 13, wherein detecting the switch status of the switch comprises:

receiving a base current level associated with a low logic state in a selected row of the switch matrix, wherein the switch is located at the intersection of the selected row and a column;

if the switch is closed, amplifying at least a portion of the base current level conducted by the column to at least the threshold current level with a transistor coupled at its base to the column and at its emitter to a scan line; and

scanning the scan line for the current signal, wherein the switch status is open if the current signal is less than the threshold current level, and wherein the switch status is closed if the current signal is at least the threshold current level.

28. (New) The method of claim 27, wherein the selected row is a first selected row, and further comprising:

before receiving the base current level in the first selected row, selecting the first selected row from a selectable plurality of rows in the switch matrix;

discontinuing to receive the base current level in the first selected row;

selecting a second selected row from the plurality of selectable rows; and

receiving the base current level in the second selected row.

29. (New) The method of claim 13, wherein the row and column configuration comprises a first row and a second row, and wherein detecting the switch status comprises:

scanning the first row of the switch matrix; and then

scanning the second row of the switch matrix.